REMARKS

This paper is being provided in conjunction with a Request for Continued Examination (RCE) and addresses points raised in a previous office action for the above-referenced application. In this amendment, Applicant has amended claims 22, 29 and 32 to clarify that which Applicant considers to be the invention. Applicant respectfully submits that the amendments to the claims are fully supported by the originally-filed specification.

Applicants thank the Examiner for allowing claim 15.

The rejection of claims 22-24 under 35 U.S.C. 112, second paragraph, has been addressed by amendments contained here to claim 22 in accordance with the guidelines as set forth in the Office Action. Applicants have clarified the connection of one of the electrodes of the first capacitor to the first node. Accordingly, Applicants respectfully request that this rejection be reconsidered and withdrawn.

The rejection of claims 22 and 23 under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,115,146 to McClure (hereinafter "McClure") is hereby traversed and reconsideration is respectfully requested in view of the amendments to the claims contained herein.

Independent claim 22, as amended herein, recites a delay circuit including first, second and third nodes. A first inverter receives a logic signal and the output of the first inverter is coupled to the first node. A second inverter is included whose input is coupled to the first node and whose output is coupled to the second node. A third inverter is included whose input is

coupled to the second node and whose output is coupled to the third node. A fourth inverter is included whose input is coupled to the third node, wherein at least one of the inverters includes a pair of transistors, a gate threshold voltage of each gate of the pair of transistors being shifted in mutually opposing directions. A first capacitor includes two electrodes, one of the electrodes connecting to a first power source line and the other connecting with a wiring layer having both ends to the first node, the wiring layer having no connection with a circuit at any points thereon between the both ends, the first capacitor being a first transistor of a first channel type. A second capacitor is coupled between the third node and the first power source line, the second capacitor being a second transistor of the first channel type. Claims 23 and 24 depend from independent claim 22.

The McClure reference discloses a power-on reset circuit for controlling test mode entry. The Office Action refers to the inverter chain and capacitors shown in the circuit illustrated in Figure 1 of McClure.

Applicant respectfully submits that McClure does teach or fairly suggest the above-noted features as claimed by Applicant. Specifically, McClure does not disclose a delay circuit in which at least one of the inverters includes a pair of transistors, a gate threshold voltage of each gate of the pair of transistors being shifted in mutually opposing directions, as is claimed by Applicant. Accordingly, Applicants respectfully request that this rejection be reconsidered and withdrawn.

The rejection of claims 22 and 24 under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,055,713 to Watanabe et al. (hereinafter "Watanabe") is hereby traversed and reconsideration is respectfully requested.

The features of independent claim 22 are discussed above. Claim 24 depends therefrom.

The Watanabe reference discloses an output circuit of an integrated circuit including first and second MOS transistors and a drive and control circuit. In Fig. 5, Watanabe discloses two inverters (I2 and I3), two capacitors (C1 and C2) and power source lines (VSS and VCC) with an output directed to a logic gate (a NAND gate-NA1); and in Figs. 7 and 11, Watanabe discloses the delay circuit with four inverters, two capacitors and a NOR gate NG.

Applicant respectfully submits that Watanabe does teach or fairly suggest the above-noted features as claimed by Applicant. Specifically, Watanabe does not disclose a delay circuit in which at least one of the inverters includes a pair of transistors, a gate threshold voltage of each gate of the pair of transistors being shifted in mutually opposing directions, as is claimed by Applicant. Accordingly, Applicants respectfully request that this rejection be reconsidered and withdrawn.

The rejection of claim 29 under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,672,990 to Chaw (hereinafter "Chaw") is hereby traversed and reconsideration is respectfully requested in view of the amendments to the claims contained herein.

Independent claim 29, as amended herein, recites delay circuit. The circuit includes 2n+1 nodes defined in series, n being a natural number, a first node receiving a logical signal and 2n inverters, each inverter arranged between adjacent nodes of said 2n+1 nodes, wherein at least one of the inverters includes a pair of transistors, a gate threshold voltage of each gate of the pair of transistors being shifted in mutually opposing directions. A capacitor of an n-MOS type is coupled between an even node and a power source line. A NOR gate is coupled to the first node and the (2n+1)th node.

The Chaw reference discloses an edge trigger pulse generator. The Office Action cites Figure 5 of Chaw in which is disclosed an inverter chain (30a and 30b) connected to a NOR gate (30c) and a capacitor coupled between a node (between inverters 30a and 30b) and ground.

Applicant respectfully submits that Chaw does teach or fairly suggest the above-noted features as claimed by Applicant. Specifically, Chaw does not disclose a delay circuit in which at least one of the inverters includes a pair of transistors, a gate threshold voltage of each gate of the pair of transistors being shifted in mutually opposing directions, as is claimed by Applicant. Accordingly, Applicants respectfully request that this rejection be reconsidered and withdrawn.

The rejection of claim 32 under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,764,090 to Yeh et al. (hereinafter "Yeh") in view of U.S. Patent No. 6,492,972 to Kubota et al. (hereinafter "Kubota") is hereby traversed and reconsideration is respectfully requested in view of the amendments to the claims contained herein.

Independent claim 32, as amended herein, recites a delay circuit receiving a logic signal having a first logical level and a second logical level. A first inverter chain includes a plurality of inverters and at least one first capacitor, the first inverter chain receiving the logic signal and the first capacitor including a MOS transistor of a first channel type. The first capacitor changes from an off-state to an on-state to increase capacitance thereof when the logic signal changes from the first logical level to the second logical level, whereby the first inverter chain outputs a first delay signal generated after a first delay time from a transition timing from the first to the second logical levels of the logic signal. The first capacitor changes from the on-state to the off-state to decrease capacitance thereof when the logic signal changes from the second logical level to the first logical level, whereby the first inverter chain outputs a second delay signal generated after a second delay time from a transition timing from the second to the first logical levels of the logic signal, the second delay time being shorter than said first delay time. A first logical gate receives the output of the first inverter chain and the logic signal. A second inverter chain includes a plurality of inverters and at least one second capacitor, the inverter chain receiving the output of the first logical gate. A second logical gate receives the output of said the logical gate and the output of the second inverter chain. A third logical gate receives the logic signal and the output of the second logical gate. At least one inverter in the first and second inverter chains includes a pair of transistors, a gate threshold voltage of each gate of the pair of transistors being shifted in mutually opposing directions, and wherein the first inverter chain and the second inverter chain have the same structure.

The Yeh reference discloses a write-control circuit for high speed static random-access-memory devices. The Office Action cites Figure 10 of Yeh as disclosing the claimed limitations except for each inverter chain further including a MOS capacitor.

The Kubota reference discloses a data signal line driving circuit and image display apparatus. The Office Action cites Figure 6A of Kubota as disclosing a capacitor connected to an inverter chain in order to increase the delay time of the inverter chain.

Applicant respectfully submits that neither Yeh nor Kubota, taken alone or in combination, teach or fairly suggest the above-noted features as claimed by Applicant. Specifically, neither Yeh nor Kubota disclose a delay circuit in which at least one of the inverters includes a pair of transistors, a gate threshold voltage of each gate of the pair of transistors being shifted in mutually opposing directions and further that the first inverter chain and the second inverter chain have the same structure (see, for example, page 26, lines 2-3 of the present specification), as is claimed by Applicant. Accordingly, Applicants respectfully request that this rejection be reconsidered and withdrawn.

Based on the above, Applicants respectfully request that the Examiner reconsider and withdraw all outstanding rejections and objections. Favorable consideration and allowance are earnestly solicited. Should there be any questions after reviewing this paper, the Examiner is invited to contact the undersigned at 617-248-4038.

Respectfully submitted,
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